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09/865,504	05/29/2001	Simon Skierszkan	11260-US	3165
23553	7590	06/06/2005	EXAMINER WARE, CICELY Q	
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DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/865,504

Applicant(s)

SKIERSZKAN ET AL.

Examiner

Cicely Ware

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on amendment filed on 12/07/2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-6,11,13,14 and 19, 20 is/are rejected.
- 7) ☒ Claim(s) 7-10,15-18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 December 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1 and 11 have been considered but are moot in view of the new ground(s) of rejection.

### ***Drawings***

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show:
  - a. Fig. 6, element 3, as on Pg. 11, line 17
  - b. Fig. 6, element 4, as on Pg. 11, line 18, as described in the specification.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as

per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

c. Fig. 8, element 5, applicant makes reference to element 5 in Fig. 8-10. Examiner suggests applicant refer consistently to element 5 as "equation" for clarification purposes.

#### ***Claim Rejections - 35 USC § 112***

3. Claims 3 and 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 3 and 4 recite "sufficiently". "Sufficiently" is vague and indefinite because it does not distinctly point out a specific frequency.

4. Claim 20 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 20 recites "a back-up signal for use in the event of failure of a principal reference signal". Examiner is unable to find support for the elements of this claim. Therefore claim 20 has not been further treated on the merits.

***Claim Objections***

5. Claims 14, 18 and 19 are objected to because of the following informalities:

a. Claim 14, line 2, applicant uses the phrase "selection one of the".

Examiner suggests applicant re-write this line for clarification purposes.

b. Claim 18, line 2, applicant uses the phrase "derived form a crystal oscillator". Examiner suggests using "derived from a crystal oscillator" for clarification purposes.

c. Claim 19, line 2, applicant uses the phrase "phase locked loop as a cut-off frequency". Examiner suggests using "phase locked loop has a cut-off frequency" for clarification purposes.

Appropriate correction is required.

6. Claims 7 and 8 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Examiner asserts that claim 7 depends on claim 6, but does not further limit claim 6.

Claim 6 recites said functional circuit is a multiplexer. However Claim 7 recites that the functional circuit of claim 6 is an adder.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3, 4, 11 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilkinson (UK Patent Application 2084415 A).

(1) With regard to claim 1, Wilkinson discloses in (Fig. 3) a timing circuit for generating clock signals, comprising: an acquisition digital phase locked loop (22) with a wide capture range for closely following an input signal (21) and with its associated disturbances; and an output digital phase locked loop (27) having a slow response relative to said acquisition phase locked loop, said output digital phase locked loop tracking a digital output of said acquisition phase locked loop to generate an output signal for the timing circuit (33); and wherein said acquisition digital phase locked loop (22) and said output phase locked loop (27) include digital low pass filters (28), said digital low pass filter(24) in said acquisition digital phase locked loop (22) having a higher cut-off frequency than said digital low pass filter (28) in said output phase locked loop (27) (Pg. 2, col. 1, lines 19-23, 44-47, col. 2, lines 68-94, 104-111, 114-118, 123-125, Pg. 3, col. 1, lines 9-25).

(2) With regard to claim 3, claim 3 inherits all the limitations of claim 1. Wilkinson further discloses wherein said digital low pass filter in said acquisition digital phase

locked loop has a high cut-off frequency to ensure that the output closely tracks the input signal and its associated error components (Pg. 3, col. 1, lines 26-43).

(3) With regard to claim 4, claim 4 inherits all the limitations of claim 3. Wilkinson further discloses wherein said digital low pass filter in said output digital phase locked loop has a low cut-off frequency to ensure that the output tracks the output of said acquisition digital phase locked loop signal without the associated error components present in the input signal (Wilkinson, Pg. 3, col. 1, lines 9-19).

(4) With regard to claim 11, claim 11 inherits all the limitations of claim 1. Wilkinson further discloses in (Fig. 3) a method of generating clock signals from an input signal subject to errors, comprising: tracking the input signal and its error components with an acquisition digital locked loop (22) to produce a digital output signal, and tracking said digital output signal with an output digital phase locked loop (27) with a slow response relative to said acquisition digital phase locked loop so as to eliminate said error components (31); and wherein said acquisition digital phase locked loop has a digital filter (24) with a high cut-off frequency relative to the cut-off frequency of a digital filter (28) in said output digital phase locked loop (27) (Pg. 2, col. 1, lines 19-23, 44-47, col. 2, lines 68-77, 81-85, 104-111, 114-118, 123-125, Pg. 3, col. 1, lines 9-25).

(5) With regard to claim 19, claim 19 inherits all the limitations of claim 1. Wilkinson further discloses wherein said filter in said acquisition phase locked loop has a cut-off frequency of a few hundred Hertz (Pg. 2, col. 2, lines 85-94).

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 5, 6, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilkinson (UK Patent Application 2084415 A) as applied to claims 1 and 11, in view of Llewellyn (US Patent 5,329,251).

(1) With regard to claim 5, claim 5 inherits all the limitations of claim 1. However Wilkinson does not disclose a plurality of said acquisition digital phase locked loops receiving respective input signals, each said acquisition digital phase locked loops being connected through a functional circuit to said output phase locked loop.

However Llewellyn discloses in (Fig. 3) a plurality of said acquisition digital phase locked loops (110, 122, 116) receiving respective input signals, each said acquisition digital phase locked loops (116, 122) being connected through a functional circuit (130) to said output phase locked loop (112, 132, 134)) (abstract, col. 3, lines 28-38, 63-68, col. 4, lines 11-17, col. 6, lines 52-54, col. 8, lines 1-3, col. 9, lines 23-30, 49-57).

Therefore it would have been obvious to one of ordinary skill in the art to modify Wilkinson to incorporate a plurality of said acquisition digital phase locked loops receiving respective input signals, each said acquisition digital phase locked loops being connected through a functional circuit to said output phase locked loop in order to quickly lock the recovered clock signal onto an extracted clock signal which has a



changing center frequency without utilizing a learning process (Llewellyn, col. 3, lines 10-13).

(2) With regard to claim 6, claim 6 inherits all the limitations of claim 5. Llewellyn further discloses in (Fig. 3) wherein said functional circuit is a multiplexer (130) to select one of the outputs of said acquisition digital phase locked loops (122, 116) (abstract, col. 3, lines 28-38, col. 6, lines 52-54, col. 9, lines 23-30, 49-57).

(3) With regard to claim 13, claim 13 inherits all the limitations of claims 11 and 5.

(4) With regard to claim 14, claim 14 inherits all the limitations of claims 13 and 6.

#### ***Allowable Subject Matter***

11. Claims 9-10, 15-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: The instant application discloses a timing circuit for generating clock signals. Prior art references show similar methods but fail to teach: **“wherein function circuit derives an output form the outputs of said acquisition digital phase locked loops according to mathematical equation”**, as in claim 9; **“wherein inputs of said acquisition digital phase locked loops are connected through respective multiplexers to a plurality of inputs and a crystal oscillator”**, as in claim 10; **“said functional circuit is an adder to combine the outputs of said acquisition digital phase locked loops to provide an average”**, as in claim 15; **“wherein said adder generates a weighted average”**, as in claim 16;

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**“wherein one of a plurality of input signals are selectable for input to each of said acquisition phase locked loops”, as in claim 17; “wherein one of said input signals is derived from a crystal oscillator for test purposes”, as in claim 18;**

### ***Conclusion***


12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 571-272-3047. The examiner can normally be reached on Monday – Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

*Cicely Ware*

cqw  
May 20, 2005

  
**STEPHEN CHIN**  
**SUPERVISORY PATENT EXAMINEE**  
**TECHNOLOGY CENTER 2600**